

RYAN SCOTT SMITH, Ph.D.

Founder, Apostate Tech, Inc.

Verified U.S. Patents, Published Patent Families, & Peer-Reviewed Publications (1996–2026)

Executive Summary of Technical Pedigree: Over a 30-year experimental physics and foundry engineering career spanning Cornell University (CESR), the University of Texas at Austin (Ph.D. under Prof. Paul S. Ho), AstroWatt Inc., GlobalFoundries, and Applied Materials, Dr. Ryan Scott Smith has authored **14 peer-reviewed journal and conference publications** (including three in *Applied Physics Letters* and first-author sub-14nm electron transport physics with IBM Fellow C.-K. Hu in *AIP Advances*) and is a named inventor on **7 Issued U.S. Patents** and **2 Additional Published U.S./International Patent Families** (9 patent families total).

Part I: Issued United States Patents (7 Granted)

1. **U.S. Patent No. 12,713,663 B2** — “Silicon super junction structures for increased voltage”

Issued: August 18, 2026 | **Assignee:** Applied Materials, Inc. (Corresponds to PCT Pub. WO 2024/173720 A1 / US 2024/0282809 A1)

Inventors: A. Nourbakhsh, R. Gaire, P. Liu, T. Sherwood, **R. S. Smith**, R. Quon, S. Krishnan.

Domain: 3D charge-balanced depletion barriers, high-aspect-ratio P–N field shaping, and breakdown control.

2. **U.S. Patent No. 12,113,020 B2** — “Formation of metal vias on metal lines”

Issued: October 8, 2024 | **Assignee:** Applied Materials, Inc. (Corresponds to Pub. US 2022/0270979 A1)

Inventors: **R. S. Smith** (First Inventor), N. Breil, K. Wu.

Domain: Selective anisotropic barrier engineering for > 300°C BEOL Tungsten (W) integration on Copper lines for CMOS Image Sensors (CIS) and analog arrays.

3. **U.S. Patent No. 11,819,847 B2** — “Nanofluidic device with silicon nitride membrane”

Issued: November 21, 2023 | **Assignee:** Applied Materials, Inc. (Corresponds to PCT Pub. WO 2022/020022 A1 / US 2022/0016628 A1)

Inventors: **R. S. Smith** (First Inventor), R. Quon, D. Collins, G. Odum, R. Sreenivasan, J. R. Johnson.

Domain: Stoichiometric low-stress Si₃N₄ dielectric membranes, electrostatic screening, and solid-state nanopore boundary transport.

4. **U.S. Patent No. 10,485,111 B2** — “Via and skip via structures”
Issued: November 19, 2019 | **Assignee:** GlobalFoundries U.S. Inc.
Domain: Multi-level M0–M3 BEOL interconnect architecture and inter-layer dielectric (ILD) capacitive optimization.
5. **U.S. Patent No. 10,199,261 B1** — “Via and skip via structures”
Issued: February 5, 2019 | **Assignee:** GlobalFoundries U.S. Inc.
Domain: Advanced-node BEOL vertical routing and thin-film dielectric barrier integration.
6. **U.S. Patent No. 10,109,526 B1** — “Etch profile control during skip via formation”
Issued: October 23, 2018 | **Assignee:** GlobalFoundries U.S. Inc.
Domain: Anisotropic dielectric etch boundary control and multi-tiered trench geometry fidelity.
7. **U.S. Patent No. 10,078,107 B2** — “Wafer level electrical test for optical proximity correction and/or etch bias”
Issued: September 18, 2018 | **Assignee:** GlobalFoundries U.S. Inc. (Corresponds to Pub. US 2017/0115337 A1)
Domain: Computational lithography (OPC) boundary verification, electrical resistor network metrology, and etch-bias compensation.

Part II: Additional Published U.S. & International Patent Families (2 Families)

1. **U.S. Pub. No. 2022/0242725 A1 / US 2022/0236250 A1 / EP 3980775 A1** —
“Manufacturing methods for dual pore sensors” & “Dual pore sensors”
Published: April–August 2022 | **Assignee:** Applied Materials, Inc.
Inventors: J. R. Johnson, R. Quon, A. Kumar, **R. S. Smith**, J. Hebding, R. Sreenivasan.
Domain: Bio-MEMS nanoscale fluidic/dielectric boundary transport and stochastic signal detection in thermal baths.
 2. **U.S. Pub. No. 2017/0052014 A1** — “Method, apparatus, and system for passive die strain measurement”
Published: February 23, 2017 | **Assignee:** GlobalFoundries U.S. Inc.
Domain: Silicon transduction of continuum mechanical and thermal package gradients.
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Part III: Peer-Reviewed Journal & Conference Publications (14 Papers)

A. Sub-14nm Electron Boundary Scattering & Chip-Package Interconnect Physics

1. **R. S. Smith**, E. T. Ryan, C.-K. Hu, K. Motoyama, N. Lanzillo, D. Metzler, L. Jiang, J. Demarest, R. Quon, L. Gignac, C. Breslin, A. Giannetta, and S. Wright, “An evaluation of Fuchs-Sondheimer and Mayadas-Shatzkes models below 14nm node wide lines,” **AIP Advances**, Vol. 9, Issue 2, p. 025015 (2019). [First-author solution of the MacDonald-Sarginson integral demonstrating negative specularity ($p = -0.2$) and boundary-scattering resistivity scaling limits below 14nm].
2. S. Gao, **R. S. Smith**, J. K. Cho, and F. Kuechenmeister, “Chip Packaging Interaction (CPI) with Cu Pillar Flip Chip for 20 nm Silicon Technology and Beyond,” **ECS Journal of Solid State Science and Technology**, Vol. 4, Issue 1, pp. N3111–N3115 (2014). [Empirical measurement of M1–M4 BEOL capacitive shifts and thermomechanical strain distributions].

B. 1 MHz Dielectric Susceptibility, Kramers-Kronig Dispersion, & Low- k Mechanics (UT Austin)

1. H. Shi, H. Huang, **R. S. Smith**, and P. S. Ho, “Characterization of Plasma Damage for Low- k Dielectric Films,” Chapter in **Metrology and Diagnostic Techniques for Nanoelectronics**, ed. Z. Ma and D. G. Seiler, Pan Stanford Publishing / CRC Press (2016).
2. **R. S. Smith**, T. Y. Tsui, and P. S. Ho, “Effect of UV radiation on ultra-low- k dielectric thin film fracture toughness and polarizability,” **Materials Chemistry and Physics**, Vol. 135, Issues 2–3, pp. 880–885 (2012).
3. **R. S. Smith**, T. Tsui, and P. S. Ho, “Analysis of Ultraviolet Curing Effect on the Dielectric Constant and Molecular Structure of a Porous Dielectric Film,” **Journal of Electronic Materials**, Vol. 39, No. 10, pp. 2337–2345 (2010).
4. H. Shi, J. Bao, **R. S. Smith**, H. Huang, J. Liu, P. S. Ho, M. L. McSwiney, M. Moinpour, and G. M. Kloster, “Origin of dielectric loss induced by oxygen plasma on organosilicate glass low- k dielectrics,” **Applied Physics Letters**, Vol. 93, Issue 19, p. 192909 (2008). [Decomposition of 1 MHz dipolar, ionic, and electronic susceptibility components via Kramers-Kronig relations].
5. H. Huang, J. Bao, J. Liu, **R. S. Smith**, Y. Sun, G. M. Kloster, M. D. Goodner, M. Moinpour, and P. S. Ho, “Dielectric Recovery of Plasma Damaged Organosilicate Low- k Films,” **MRS Proceedings**, Vol. 1079 (2008).

6. **R. S. Smith**, T. Tsui, and P. S. Ho, “The Effect of Ultraviolet Light Curing on the Material and Fracture Properties of a $k \sim 2.5$ Low- k Dielectric,” **MRS Proceedings**, Vol. 990 (2007).

C. Silicon P–I–N Heterojunctions & Thermomechanical Spalling (AstroWatt / UT Austin)

1. E. U. Onyegam, D. Sarkar, M. M. Hilali, S. Saha, L. Mathew, R. A. Rao, **R. S. Smith**, D. Xu, D. Jawarani, R. Garcia, M. Ainom, and S. K. Banerjee, “Realization of dual-heterojunction solar cells on ultra-thin $\sim 25 \mu\text{m}$, flexible silicon substrates,” **Applied Physics Letters**, Vol. 104, Issue 15, p. 153902 (2014).
2. S. Saha, M. M. Hilali, E. U. Onyegam, D. Sarkar, D. Jawarani, R. A. Rao, L. Mathew, **R. S. Smith**, D. Xu, U. K. Das, B. Sopori, and S. K. Banerjee, “Single heterojunction solar cells on exfoliated flexible $\sim 25 \mu\text{m}$ thick mono-crystalline silicon substrates,” **Applied Physics Letters**, Vol. 102, Issue 16, p. 163904 (2013).
3. D. Xu, P. S. Ho, R. A. Rao, L. Mathew, **R. S. Smith**, S. Saha, D. Sarkar, C. Vass, and D. Jawarani, “Mechanical Strength and Reliability of a Novel Thin Monocrystalline Silicon Solar Cell,” **2012 IEEE International Reliability Physics Symposium (IRPS)**, pp. 4A.3.1–4A.3.6 (2012).
4. S. Saha, M. M. Hilali, E. U. Onyegam, D. Sarkar, R. A. Rao, L. Mathew, **R. S. Smith**, D. Xu, D. Jawarani, R. Garcia, and S. K. Banerjee, “Remote Plasma Chemical Vapor Deposition for High Efficiency Ultra Thin ~ 25 Microns Crystalline Si Solar Cells,” **38th IEEE Photovoltaic Specialists Conference (PVSC)**, pp. 001001–001004 (2012).

D. Early Relativistic Beam Optics & Atomic Coincidence Physics (Cornell & UNT)

1. **R. S. Smith**, S. Henderson, D. Hartill, T. Chen, and R. H. Siemann (Cornell Electron Storage Ring, Laboratory of Nuclear Studies), “A turn-by-turn vertical profile monitor,” **Proceedings of the 1997 IEEE Particle Accelerator Conference (PAC '97)**, Vol. 2, pp. 2152–2154 (1997). [First-author high-speed optical fiber and detector array for real-time relativistic electron bunch phase-space profiling].
 2. B. R. Chalamala, C. T. Newell, **R. S. Smith**, Y. Zhang, and D. E. Golden (University of North Texas), “Apparatus for Studying Electron-Impact Ionization of Ions Using Multiparameter Coincidence Techniques,” **AIP Conference Proceedings**, Vol. 392, pp. 197–200 (1997). [Simultaneous momentum-vector coincidence detection in multi-particle phase space].
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Notice on Intellectual Property & Freedom-to-Operate: All patents and publications listed above represent prior academic and corporate research assigned to their respective institutions (Cornell University, The University of Texas at Austin, AstroWatt Inc., GlobalFoundries U.S. Inc., and Applied Materials, Inc.) and are provided strictly as a historical record of the founder's scientific training and foundry engineering qualifications. The **Apostate Tech Thermodynamic Vector Architecture** was conceived and derived independently in 2026 and requires **zero proprietary advanced-node unit-process recipes**, executing natively on standard, public-domain 65nm–130nm planar SOI and CIS foundry design rules.